Notice of Allowability	Application No.	Applicant(s)	
	10/691,530	KER ET AL.	
	Examiner	Art Unit	
	Abbas I. Abdulselam	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/08/05*.

2. ☒ The allowed claim(s) is/are *1-18*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

RICHARD HUERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

DETAILED ACTION

REASONS FOL ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

Takeshi (JP 2002-280895) teaches a level shifter circuit, provided with a current mirror circuit 11 which has a transistor having a prescribed threshold for converting the input signal of low amplitude to the output signal of high amplitude, a circuit composed of source follower circuits 12a and 12b and current source transistor circuits 13a and 13b for adding offset to the input signal and supplying it to the current mirror circuit 11, and bias varying circuits 14a and 14b for changing bias for determining offset to be added based on the input signal and supplying it to the current source transistor circuits 13a and 13b (see the abstract).

Bertin et al. (USPN 6222395) teach a voltage control means connected to the substrates of a first and a second transistors for adjusting the threshold voltage of the first and the second transistors to be at different values, thereby adjusting the value of the reference voltage Vref (col. 2, lines 5-22).

Regarding claim 1, the prior art does not teach a level shifter for use in thin film transistor liquid crystal displays (TFT-LCD), comprising: a shift circuit for shifting from an input voltage level to an output voltage level, comprising: a first transistor comprising a source, a drain, a gate, and a body; and a second transistor comprising a source, a drain, a gate, and a body; and a first bias circuit, comprising an input terminal and an output terminal; wherein the output terminal of

the first bias circuit is connected to the body of the first transistor to adjust a threshold voltage of the first transistor according to the input voltage level.

Regarding claim 8, the prior art does not teach a level shifter for use in TFT-LCDs, comprising: a shift circuit for shifting from an input voltage level to an output voltage level, comprising: a first transistor being a n-channel TFT and comprising a source, a drain, a gate, and a body; a second transistor being a n-channel TFT and comprising a source, a drain, a gate, and a body; a third transistor being a p-channel TFT and comprising a source, a drain, and a gate; and a fourth transistor being a p-channel TFT and comprising a source, a drain, and a gate; and a first bias circuit, comprising an input terminal and an output terminal; wherein the output terminal of the first bias circuit is connected to the body of the first transistor to adjust a threshold voltage of the first transistor according to the input voltage level.

Regarding claim 14, the prior art does not teach a level shifter for use in TFT-LCDs, comprising: a first input terminal for inputting the input voltage level; a second input terminal for inputting the input voltage level but with opposite phase; a shift circuit for shifting from an input voltage level to an output voltage level, comprising: a first transistor being a n-channel TFT and comprising a source, a drain, a gate, and a body; a second transistor being a n-channel TFT and comprising a source, a drain, a gate, and a body; a third transistor being a p-channel TFT and comprising a source, a drain, and a gate; and a fourth transistor being a p-channel TFT and comprising a source, a drain, and a gate; a first bias circuit, comprising an input terminal and an output terminal, for biasing the body of the first transistor; and a second bias circuit, comprising

an input terminal and an output terminal, for biasing the body of the second transistor; wherein the input terminal of the first bias circuit is connected to the gate of the first transistor, the input terminal of the second bias circuit is connected to the gate of the second transistor, the output terminal of the first bias circuit is connected to the body of the first transistor, the output terminal of the second bias circuit is connected to the body of the second transistor, the gate of the first transistor is connected to the first input terminal, and the gate of the second transistor is connected to the second input terminal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulselam whose telephone number is 571-272-7685. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abbas Abdulselam

Examiner

Art Unit 2629

June 15, 2006

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600